PGY-I3C-EX-PD

I3C Exerciser and Protocol Analyzer

The I3C serial bus interface is emerging as a chosen interface for all future sensor connectivity in mobile phone and automotive Industries. This could also be chosen as a low-cost, reliable interface for future embedded electronic applications to address the new data-intensive applications.

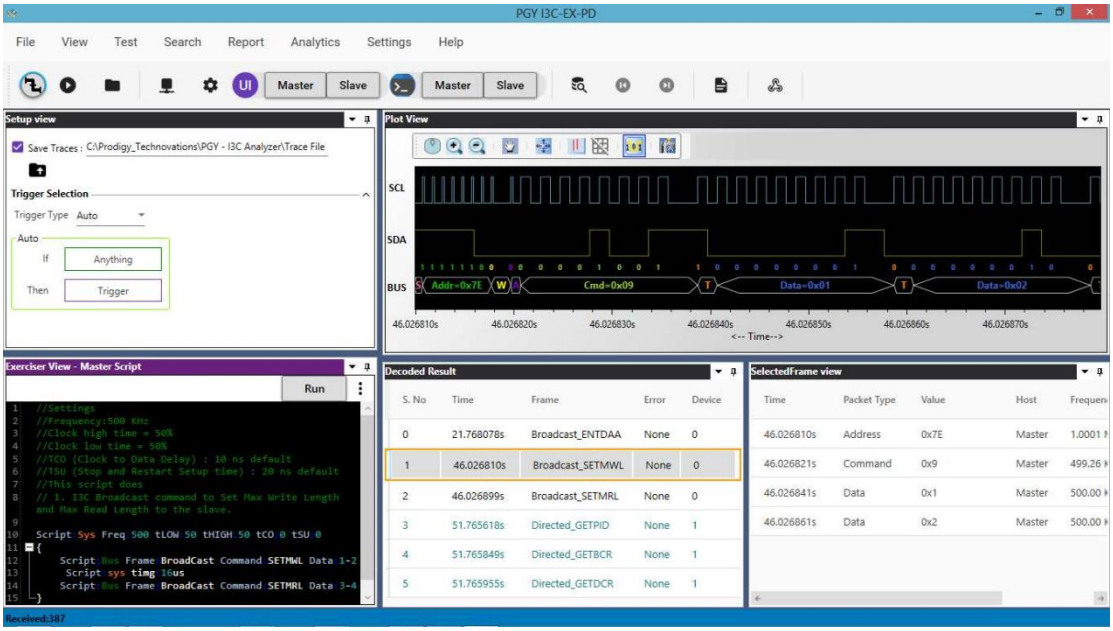
The PGY-I3C-EX-PD is the leading instrument that enables the design and test engineers to test the I3C designs for its specifications by configuring the PGY-I3C-EX-PD as Master/Slave to generate I3C traffic with error injection capabilities and to decode I3C protocol packets.

Key Features

- Supports v1.0/v1.1 Specifications[1].
- Ability to configure it as Master or Slave.
- Ability to configure BCR, LVR and DCR registers.
- Simultaneously generate I3C traffic and Protocol decode of the Bus.
- Optional Compliance Test Specifications (CTS) test script support.
- Supports legacy I2C slaves and Master.
- Generate different I3C SDR and HDR Packets.
- Supports IBI and Hot Plug capabilities.
- Error Injection such CRC errors, parity errors and ACK/NACK errors.
- Variable I3C data speeds and duty cycle.
- PMIC device support as per JEDEC DDR5 spec requirement.
- Margin test capability: Voltage and timing variation.
- Continuous streaming of protocol data between instrument and host computer.
- Timing diagram of Protocol decoded bus.
- Listing view of Protocol activity.
- Error Analysis in Protocol Decode.
- Ability to write exerciser script to combine multiple data frame generation at different data speeds.
- USB2/3 host computer interface.
- API support for automation in Python or C++.

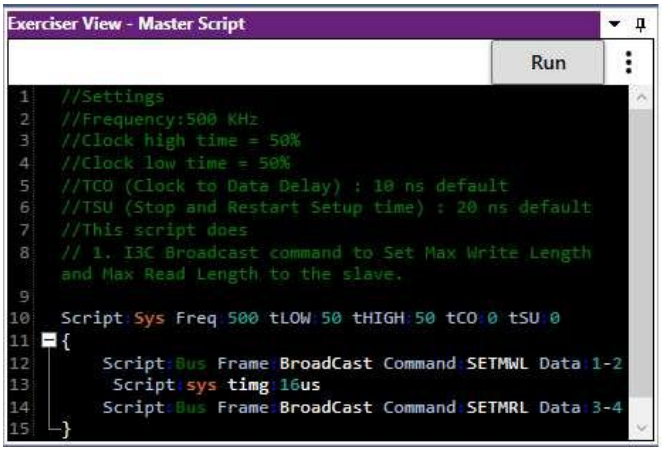
[1] v1.1 supports only one lane commands

Multi-Domain view



Multi-domain View provides the complete view of I3C Protocol activity in a single GUI. Users can easily set up the analyzer to generate I3C/I2C traffic using the GUI or script. Users can set different trigger conditions from the setup menu to capture protocol activity at specific events and decode the transition between the Master and Slave. The decoded results can be viewed in the timing diagram and protocol listing windows with auto-correlation. State machine view provides switching of state machine between master and slave for design validation. This comprehensive view of information makes it an industry-best offering and an easy-to-use solution to debug the I3C protocol activity.

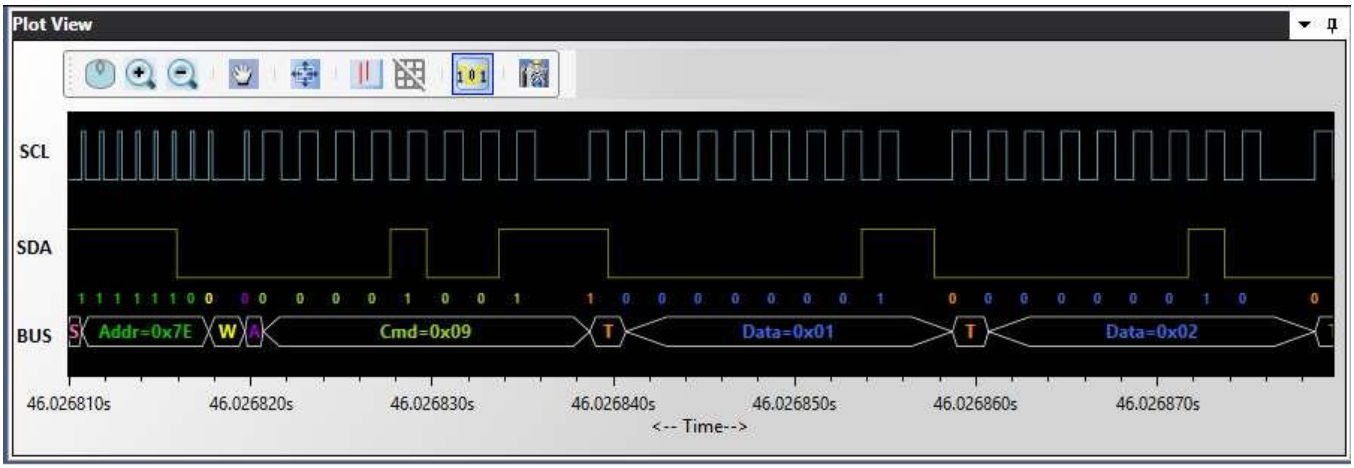
Exerciser



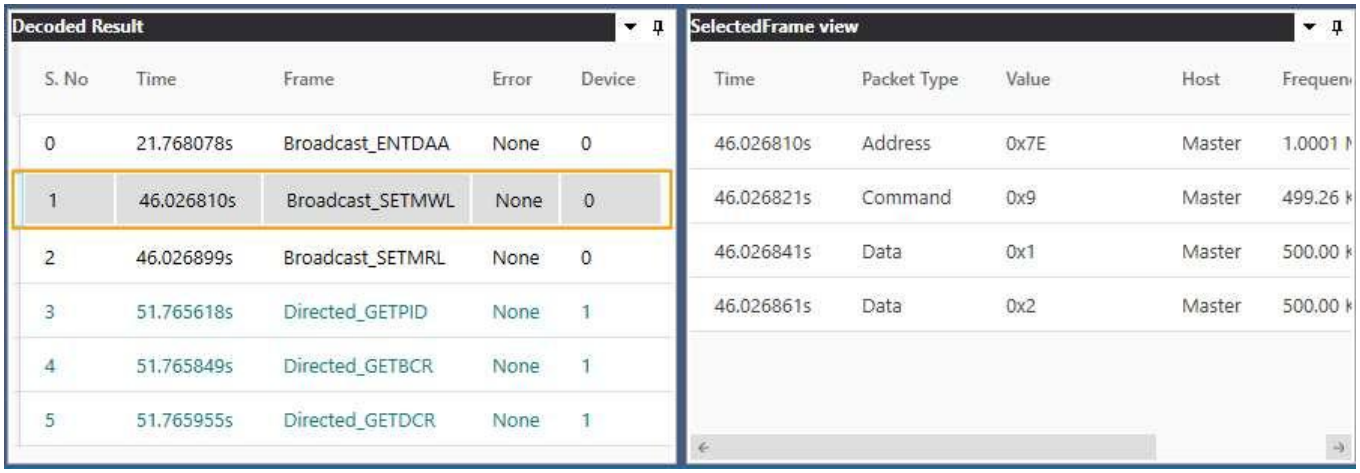
PGY-I3C-EX-PD supports I3C traffic generation using GUI and Script. Users can perform simple traffic generation using the GUI to test the DUT. Script-based GUI provides flexibility to emulate the complete expected traffic in the real-world including error injections. In the below sample script users can generate I3C traffic as below:

Script line #10: Set system Frequency 500KHz, Duty cycle to 50%, CLK to data delay to 10ns (default), start to restart setup time to 20ns (default)
Script line #12: SETMWL
Script line #13: Set system inter message gap to 16us
Script line #14: SETMRL

Timing Diagram and Protocol Listing View

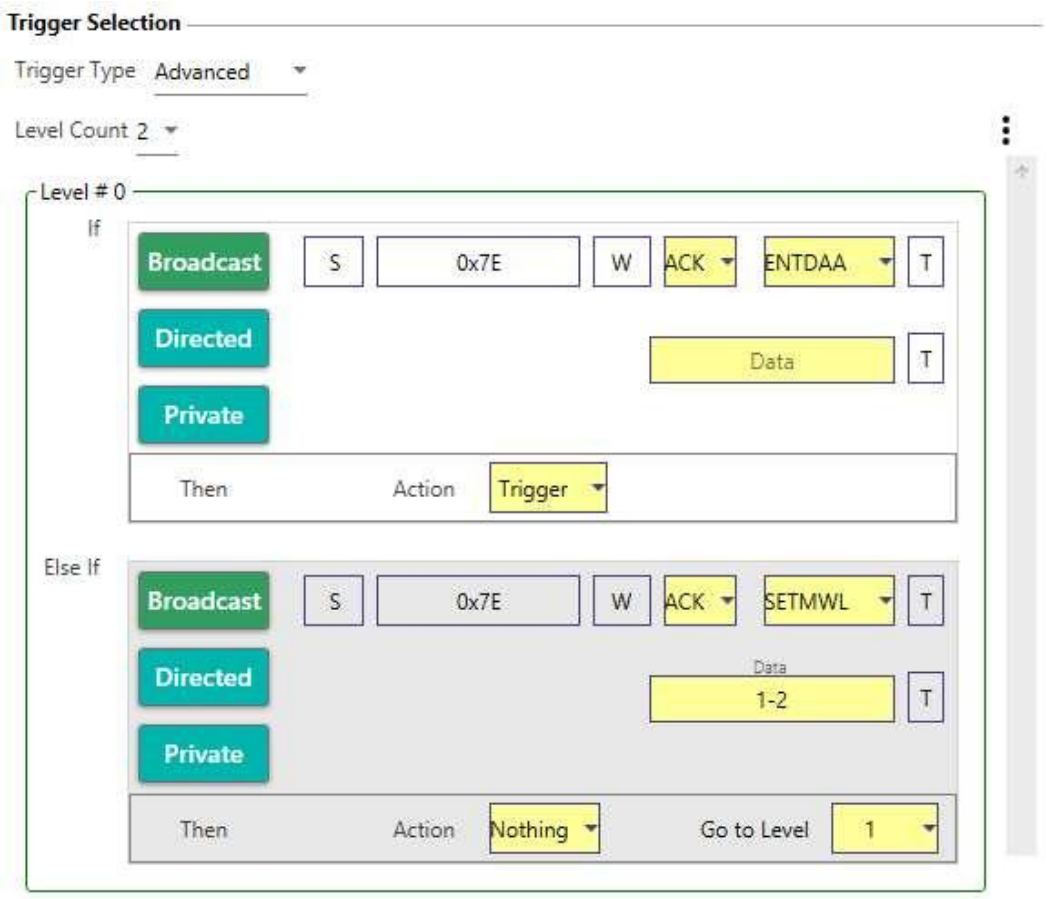


The timing view provides the plot of SCL and SDA signals with bus diagram information. Overlaying of protocol bits on the digital timing waveform helps in the easy debugging of protocol decoded data. Cursor and Zoom features make it convenient to analyze protocol in timing diagrams for any timing error



The protocol window provides the decoded packet information in each state and all packet details with error info in the packet. The selected frame in the protocol listing window will be auto-correlated in the timing view to view the timing information of the packet.

Powerful Trigger Capabilities



PGY-I3C-EX-PD supports auto, simple, and advanced trigger capabilities. The analyzer can trigger on any of the protocol packets such as broadcast, directed, or private messages. Advanced trigger provides the flexibility to monitor multiple trigger conditions and can set multiple state trigger machines.

PGY-I3C Specifications	Features
Exerciser:	
Configurable	1 Master + 3 Slaves or 1 Secondary Master + 2 Slaves
I3C / I2C Traffic Generation	Custom I3C / I2C traffic generation (Simulate real world network traffic)
SCL Frequency	1Hz to 12.5MHz **Note**: Prodigy device supports up to 10MHz at 1V frequency as a slave
Configurable Voltage Level Drive	0.9V to 3.4V Steps: 0.9 – 1.27 V (In steps of 5mV) 1.27 – 1.95V (In steps of 10mV) 1.95 - 3.4V (In steps of 30mV)
Hot Join	Yes, supported
IBI	Yes, supported
CCC Support	All CCC are supported in Master slide. All CCC are supported in Slave except SETXTIME, ENTTM, ENTAS*
SCL Duty Cycle variation	User Defined (In Fine resolutions of 10ns)
SCL & SDA Delay	User Defined (In Fine resolutions of 18ps)
Delay between two messages	User Defined (In Fine resolutions of ns, us, ms and seconds)
Error injection	S0 to S5 types of errors specified in I3C specifications. CRC errors in DDR traffic. Preamble errors in DDR traffic ACK / NACK Errors (Slave) Master Abort. Non-Standard Frames. Non-Standard Start, Stop and HDR exit patterns, slave reset Save and Load Scripts.
API Support	Support for Automation of operation using Python or C++
Protocol Analysis:	
Supports	I3C & I2C protocol decode
Protocol Views	Timing Diagram View Protocol Listing View Bus-Diagram to display Protocol packets with timing diagram plot
Protocol Trigger	Auto (Trigger on any packet) Simple (Trigger on user defined I3C or I2C packet) Advanced (Multi-state & multi-level trigger with timer capability)
Capture Duration	Continuous streaming Protocol Data to host HDD/SSD
Protocol Error Report	S0 to S5 types of errors specified in the I3C specifications CRC errors in DDR traffic Preamble errors in DDR traffic ACK /NACK Errors (Slave) Master Abort Non-Standard frames Non-standard Start, Stop and HDR exit patterns.
Host Connectivity	USB 3.0 / 2.0 interface

Ordering Information

PGY-I3C-EX-PD (v 1.0): I3C Protocol Exerciser and Analyzer (supports v 1.0 specifications).
PGY-I3C-EX-PD (v 1.1): I3C Protocol Exerciser and Analyzer (supports v 1.1 specifications).
Opt CTS (v1.1): Compliance test specifications for v 1.1 specifications.
PGY-I3C-UPG (v1.0 to v 1.1): Upgrade Option from version 1.0 to version 1.1 specifications.

Deliverables for PGY-I3C-EX-PD

PGY-I3C-EX-PD Unit.
USB 3.0 Cable.
PGY-I3C-EX-PD Software in CD.
12V DC Adapter.
Flying lead probe cable with female connector to connect to DUT.

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About Prodigy Technovations Pvt Ltd

Prodigy Technovations Pvt Ltd (www.prodigytechno.com) is a leading global technology provider of Protocol Decode, and Physical layer testing solutions on test and measurement equipment. The company's ongoing efforts include successful implementation of innovative and comprehensive protocol decode and physical layer testing solutions that span the serial data, telecommunications, automotive, and defense electronics sectors worldwide.